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Application Number	10/788,700
Filing Date	February 27, 2004
First Named Inventor	Sidgata V. Sreenivasan
Art Unit	Unassigned
Examiner Name	Unassigned
Attorney Docket Number	P107-49-03

Total Number of Pages in This Submission

ENCLOSURES (Check all that apply)

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<input type="checkbox"/> Affidavits/declaration(s)	<input type="checkbox"/> Power of Attorney, Revocation	<input type="checkbox"/> Status Letter
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This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Sreenivasan et al. PATENT APPLICATION
Serial No.: 10/788,700 Group Art Unit: Unassigned
Filing Date: February 27, 2004 Examiner: Unassigned
For: FULL WAFER OR LARGE AREA IMPRINTING WITH MULTIPLE
SEPARATED SUB-FIELDS FOR HIGH THROUGHPUT LITHOGRAPHY

INFORMATION DISCLOSURE STATEMENT

Commissioner
for Patents
Alexandria, VA 22313

Sir:

The following information is submitted in compliance with Applicants' duty of disclosure under 37 C.F.R. § 1.56.

Form PTO-1449 and a copy of each reference recited below accompanies this document. It is respectfully requested that the cited information be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom.

ISSUED PATENTS

<u>Patent Number</u>	<u>Inventor</u>	<u>Grant Date</u>
4,724,222	Feldman	02/09/1988
4,731,155	Napoli et al.	03/15/1988
5,425,848	Haisma et al.	06/20/1995
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6,309,580	Chou	10/30/2001
6,334,960	Willson et al.	01/01/2002
6,518,168	Clem et al.	02/11/2003
6,696,220	Bailey et al.	02/24/2004

PENDING PATENT APPLICATIONS

<u>Serial Number</u>	<u>Inventor</u>	<u>Filing Date</u>
09/698,317	Choi et al.	10/27/2000
10/136,188	Voisin	05/01/2002
10/194,414	Sreenivasan et al.	07/11/2002
10/194,991	Sreenivasan et al.	07/11/2002
10/293,224	Choi et al.	11/13/2002
10/293,919	Voisin	11/13/2002
10/316,963	Choi et al.	12/11/2002
10/614,716	Choi et al.	07/7/2003
10/735,110	Nimmakayala et al.	12/12/2003
10/780,821	Sreenivasan et al.	01/20/2004

PATENT APPLICATION PUBLICATIONS

<u>Publication No.</u>	<u>Inventor</u>	<u>Publication Date</u>
US 2002/0098426	Sreenivasan et al.	07-25-2002
US 2002/0094496	Choi et al.	07-18-2002
US 2003/0093122	Choi et al.	07-18-2002

FOREIGN PATENT DOCUMENTS

<u>Document Number</u>	<u>Inventor</u>	<u>Pub. Date</u>
DE 2800476	Lamprecht et al.	07/13/1978
JP 1-196749	Matsumoto et al.	08/08/1989
WO 01/69317	Montelius et al.	09/20/2001
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NON-PATENT DOCUMENTS

Krug, Herbert et al. "Fine Patterning of Thin Sol-Gel Films,"
Journal of Non-Crystalline Solids, 1992, 447-450.

Krauss, et al. "Fabrication of Nanodevices Using Sub-25nm
Imprint Lithography," Appl. Phys. Lett., 67(21), 3114-
3116, 1995.

- Chou et al. "Imprint of Sub-25 nm Vias and Trenches in Polymers," Applied Physics Letters, 67(21), pp. 3114-3116, 1995.
- Chou et al. "Imprint Lithography with 25-Nanometer Resolution," Science, vol. 272, Apr. 5, 1996, pp. 85-87.
- Haisma, J. et al. "Mold-Assisted Nanolithography: A Process for Reliable Pattern Replication," Journal of Vacuum Science and Technology, 1996, 14, 4124-4128.
- Chou et al. "Imprint Lithography with Sub-10 nm Feature Size and High Throughput", Microelectronic Engineering 35, 1997, 237-240.
- Feldman et al., "Wafer Chuck for Magnification Correction in X-ray Lithography," American Vacuum Society, 1998, pp. 3476-3479.
- Scheer, H.C. et al. "Problems of Nanoimprinting Technique for Nanometer Scale Pattern Definition," Journal of Vacuum Science and Technology, 1998, 16, 3917-3921.
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- Chou, Stephen et al. "Lithographically-induced Self Assembly of Periodic Micropillar Arrays," Journal of Vacuum Science and Technology, 1999, 17, 3197-3202.
- Ruchhoeft, P. et al. "Patterning Curved Surfaces: Template Generation by Ion Beam Proximity Lithography and Relief Transfer by Step and Flash Imprint Lithography," Journal of Vacuum Science and Technology, 1999, 17, 2965-2982.
- Choi, B.J. et al. "Design of Orientation Stages for Step and Flash Imprint Lithography," Precision Engineering, 2001, 25, 192-199.

Otto M. et al., "Step and Repeat UV-Nanoimprint Lithography: Material Issues," Nanoimprint and Nanoimprint Technology Conference, San Francisco, December 11-13, 2002.

Johnson et al., "Advances in Step and Flash Imprint Lithography," SPIE Microlithography Conference, February 23-28, 2003.

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Date: March 31, 2004

Respectfully,



Kenneth C. Brooks
Reg. No. 38393

P.O. Box 10417
Austin, Texas 78766-1417
Telephone: 512-527-0104
Facsimile: 512-527-0107
patentsrus@earthlink.net

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5

Application Number

10/788.700

Filing Date

02/27/2004

First Named Inventor

Sreenivasan

Group Art Unit

Unassigned

Examiner Name

Unassigned

Attorney Docket Number

P107/MII-72-54-03

U.S. PATENT DOCUMENTS

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of

5

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Application Number

10/788,700

Filing Date

02/27/2004

First Named Inventor

Sreenivasan

Group Art Unit

Unassigned

Examiner Name

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Attorney Docket Number

P107/MII-72-54-03

FOREIGN PATENT DOCUMENTS

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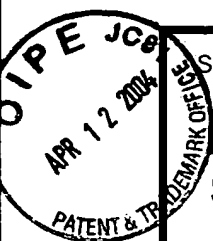
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Application Number	10/788,700
Filing Date	02/27/2004
First Named Inventor	Sreenivasan
Group Art Unit	Unassigned
Examiner Name	Unassigned
Attorney Docket Number	P107/MII-72-54-03

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	A18	KRUG et al., "Fine Patterning of Thin Sol-Gel Films," Journal of Non-Crystalline Solids, 1992, pp. 447-450, vol. 147 & 148.	
	A19	Krauss et al., "Fabrication of Nanodevices Using Sub-25nm Imprint Lithography," Appl. Phys. Lett 67(21), 3114-3116, 1995	
	A20	CHOU et al., "Imprint of Sub-25 nm Vias and Trenches in Polymers," Applied Physics Letters, November 20, 1995, pp. 3114-3116, vol. 67(21).	
	A21	CHOU et al., "Imprint Lithography with 25-Nanometer Resolution," Science, Apr. 5, 1996, pp. 85-87, vol. 272.	
	A22	HAISMA et al., "Mold-Assisted Nanolithography: A Process for Reliable Pattern Replication," Journal of Vacuum Science and Technology, Nov/Dec 1996, pp. 4124-4128, vol. B 14(6).	
	A23	CHOU et al., "Imprint Lithography with Sub-10nm Feature Size and High Throughput," Microelectronic Engineering, 1997, pp. 237-240, vol. 35.	
	A24	FELDMAN et al., "Wafer chuck for manification correction in x-ray lithography," American Vacuum Society, 1998, pp. 3476-3479.	
	A25	SCHEER et al., "Problems of the Nanoimprinting Technique for Nanometer Scale Pattern Definition," Journal of Vacuum Science and Technology, Nov/Dec 1998, pp. 3917-3921, vol. B 16(6).	
	A26	COLBURN. et al., "Step and Flash Imprint Lithography: A New Approach to High-Resolution Patterning", Proc. of SPIE, 1999, pp. 379-389, vol. 3676.	
	A27	CHOU et al., "Lithographically-Induced Self Assembly of Periodic Polymer Micropillar Arrays," Journal of Vacuum Science and Technology, Nov/Dec 1999, pp. 3197-3202, vol. B 17(6).	
	A28	RUCHHOEFT et al., "Patterning Curved Surfaces: Template Generation by Ion Beam Proximity Lithography and Relief Transfer by Step and Flash Imprint Lithography," Journal of Vacuum Science and Technology, 1999, pp. 2965-2982, vol. 17.	

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				First Named Inventor	Sreenivasan
				Group Art Unit	Unassigned
				Examiner Name	Unassigned
Sheet	4	of	5	Attorney Docket Number	P107/MII-72-54-03

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	A29	CHOI et al., "Design of Orientation Stages for Step and Flash Imprint Lithography," Precision Engineering, Journal of the International Societies for Precision Engineering and Nanotechnology, 2001, pp. 192-199, vol. 25.	
	A30	CHOI et al., "High Precision Orientation Alignment and Gap Control Stages for Imprint Lithography Processes," U.S. Patent Application 09/698,317. Filed with USPTO on October 27, 2000.	
	A31	SREENIVASAN et al., "High-Resolution Overlay Alignment Methods and Systems for Imprint Lithography," U.S. Patent Application Publication 2002/0098426. Published on July 25, 2002.	
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	A33	CHOI et al., "Methods for High-Precision Gap and Orientation Sensing Between a Transparent Template and Substrate for Imprint Lithography," U.S. Patent Application Publication 2003/0093122. Published on July 18, 2002.	
	A34	VOISIN, "Methods of Manufacturing a Lithography Template," U.S. Patent Application 10/136,188, Filed with USPTO on May 1, 2002.	
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	A36	SREENIVASAN et al., "Step and Repeat Imprint Lithography Processes," U.S. Patent Application 10/194,991. Filed with USPTO July 11, 2002.	
	A37	OTTO M. et al., "Step and Repeat UV-Nanoimprint Lithography: Material Issues," Nanoimprint and Nanoprint Technology Conference, San Francisco, December 11-13, 2002.	
	A38	JOHNSON, et al., "Advances in Step and Flash Imprint Lithography," SPIE Microlithography Conference, February 23-28, 2003.	
	A39	CHOI et al., "A Chucking System and Method for Modulating Shapes of Substrates," U.S. Patent Application 10/293,224. Filed with USPTO on November 13, 2002.	

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First Named Inventor	Sreenivasan
Group Art Unit	Unassigned
Examiner Name	Unassigned
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	A40	VOISIN, "Methods of Inspecting A Lithography Template," U.S. Patent Application 10/293,919. Filed with USPTO on November 13, 2002	
	A41	CHOI et al., "A Method For Modulating Shapes of Substrates," U.S. Patent Application 10/316,963. Filed with USPTO on December 11, 2002.	
	A42	CHOI et al., "A Conforming Template For Patterning Liquids Disposed On Substrates," U.S. Patent Application 10/614,716. Filed with USPTO on July 7, 2003.	
	A43	NIMMAKAYALA et al., "Magnification Correction Employing Out-of-Plane Distortion of a Substrate," U.S. Patent Application 10/735,110. Filed with USPTO on December 12, 2003.	
	A44	SREENIVASAN et al., "Method for Concurrently Employing Differing Materials to Form a Layer on a Substrate," U.S. Patent Application 10/780,821. Filed with USPTO on January 20, 2004.	

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